PCT

(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
105029

U.S. APPLICATION NO.
(if known, sec 37 C.F.R.1.5)
09/486556

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/03417	June 25, 1999	July 1, 1998

TITLE OF INVENTION
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

APPLICANT(S) FOR DO/EO/US
Nobuaki HASHIMOTO

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A small entity statement.

16. ☐ Other items or information:

Rec'd PCT/PTO 29 FEB 2000

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 09/486556	INTERNATIONAL APPLICATION NO. PCT/JP99/03417	ATTORNEY'S DOCKET NUMBER 105029

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO.....$840.00 International preliminary examination fee paid to USPTO (37 CFR1.482).....$670.00 No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)).....$690.00 Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....$970.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	29- 20 =	9	X $ 18.00	$ 162.00	
Independent Claims	2- 3 =	0	X $ 78.00	$	
Multiple dependent claim(s)(if applicable)			+ $260.00	$	
TOTAL OF ABOVE CALCULATIONS =				$1002.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28). -				$	
SUBTOTAL =				$1002.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 month from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$1002.00	
				Amount to be refunded	$
				Charged	$

a. ☒ Check No. 106609 in the amount of $1,002.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320

NAME: James A. Oliff
REGISTRATION NUMBER: 27,075

NAME: Thomas J. Pardini
REGISTRATION NUMBER: 30,411

(1390 Rev.8-93)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: U.S. National Stage of PCT/JP99/03417

Filed: February 29, 2000 Docket No.: 105029

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 27 and 28 as follows:

Claim 27, line 2, change "any of claims 1 to 20" to --claim 1--.

Claim 28, line 2, change "any of claims 21 to 26" to --claim 21--.

REMARKS

Claims 1-29 are pending. By this Preliminary Amendment, claims 27 and 28 are amended to eliminate multiple dependencies. Prompt and favorable examination on the merits is respectfully solicited.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Thomas J. Pardini
Registration No. 30,411

JAO:TJP/kmc

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

TECHNICAL FIELD

The present invention relates to a semiconductor device and method of manufacture thereof, and to a circuit board and an electronic instrument.

BACKGROUND ART

In recent years, with the increasing compactness of electronic instruments, semiconductor device packages adapted to high density mounting are in demand. In response to this, surface mounting packages such as a ball grid array (BGA) and a chip scale/size package (CSP) have been developed. In a surface mounting package, a substrate may be used which has formed thereon an interconnect pattern for connection to a semiconductor chip.

In a conventional surface mounting package, since it is difficult to provide a protective film for protecting without gaps an interconnect pattern and so forth, it has been difficult to improve productivity.

The present invention solves this problem, and has as its objective the provision of a method of manufacturing a semiconductor device and a semiconductor device manufactured by said method, of a circuit board and of an electronic instrument, having excellent reliability and productivity.

DISCLOSURE OF THE INVENTION

(1) A method of manufacturing a semiconductor device of the present invention is a method in which a semiconductor chip on which electrodes are formed, and a substrate on which an interconnect pattern is formed and which is covered by a protective layer except a region in the interconnect pattern of electrical connection with the electrodes, are connected by an adhesive. This method of manufacturing a semiconductor comprises:

a first step of providing the adhesive on the substrate from a region of mounting of the semiconductor chip to the protective layer, between the interconnect pattern and the electrodes; and

a second step of adhering the substrate to the semiconductor chip by means of the adhesive to electrically connect the interconnect pattern with the electrodes.

According to this aspect of the invention, since the adhesive is provided to extend over the protective layer, no gap is formed between the adhesive and the protective layer, the interconnect pattern is not exposed, and migration can be prevented.

(2) In this method of manufacturing a semiconductor device, the interconnect pattern and the electrodes may be electrically connected by conductive particles dispersed in the adhesive.

By means of this, since the interconnect pattern and electrodes are electrically connected by the conductive

particles, a semiconductor device can be manufactured by a method of excellent reliability and productivity.

(3) In this method of manufacturing a semiconductor device, before the first step, the adhesive may be previously disposed on the surface of the semiconductor chip on which the electrodes are formed.

(4) In this method of manufacturing a semiconductor device, before the first step, the adhesive may be previously disposed on the surface of the substrate on which the interconnect pattern is formed.

(5) In this method of manufacturing a semiconductor device, the adhesive may be a thermosetting adhesive.

(6) In this method of manufacturing a semiconductor device, the adhesive may be spread out beyond the semiconductor chip in the first step; and heat may be applied between the semiconductor chip and the substrate to cure the adhesive between the semiconductor chip and the substrate in the second step; and this method of manufacturing a semiconductor device may further comprise a third step of applying heat to a part of the adhesive not completely cured in the second step.

(7) In this method of manufacturing a semiconductor device, the adhesive may be heated by means of a heating jig in the third step.

(8) In this method of manufacturing a semiconductor device, a nonadhesive layer having improved nonadhesive properties with respect to the adhesive may be interposed between the heating jig and the adhesive, before heating the

adhesive.

(9) In this method of manufacturing a semiconductor device, the nonadhesive layer may be provided on the heating jig.

(10) In this method of manufacturing a semiconductor device, the nonadhesive layer may be provided on the adhesive.

(11) In this method of manufacturing a semiconductor device, the adhesive may be heated by a non-contact method in the third step.

(12) This method of manufacturing a semiconductor device may further comprise a reflow step of forming solder balls on the substrate to be connected to the interconnect pattern, wherein the third step is carried out in this reflow step.

(13) This method of manufacturing a semiconductor device may further comprise a reflow step of electrically connecting an electronic component other than the semiconductor chip to the interconnect pattern, wherein the third step is carried out in this reflow step.

(14) In this method of manufacturing a semiconductor device, the substrate may be cut together with the adhesive in a region not in contact with the semiconductor chip, after the second step.

(15) In this method of manufacturing a semiconductor device, the substrate may be cut in a region outside the edge of the interconnect pattern.

(16) In this method of manufacturing a semiconductor device, the whole of the adhesive may be cured before the

substrate is cut together with the cured adhesive.

(17) In this method of manufacturing a semiconductor device, the adhesive may be caused to surround at least a part of a lateral surface of the semiconductor chip in the second step.

By means of this, since the adhesive covers at least a part of the lateral surface of the semiconductor chip, the semiconductor chip can be protected from mechanical damage, and also water is rendered unable to reach the electrodes, and corrosion can be prevented.

(18) In this method of manufacturing a semiconductor device, the adhesive may be provided in the first step at a thickness greater than the interval between the semiconductor chip and the substrate after the second step, and may be spread out beyond the semiconductor chip by applying pressure between the semiconductor chip and the substrate in the second step.

(19) In this method of manufacturing a semiconductor device, the adhesive may include a shading material.

By means of this, since the adhesive includes a shading material, light can be prevented from reaching the surface of the semiconductor chip having the electrodes. Therefore, malfunction of the semiconductor chip can be prevented.

(20) In this method of manufacturing a semiconductor device, the substrate may be provided previously covered by the protective layer except a region of mounting of the semiconductor chip and the periphery of the mounting region.

(21) A semiconductor device according to the present

invention comprises: a semiconductor chip having electrodes; a substrate on which an interconnect pattern is formed; a protective layer provided on the substrate excluding a region of the interconnect pattern of electrical connection with the electrodes of the semiconductor chip; and an adhesive;

wherein the adhesive is provided on the substrate from a region of mounting of the semiconductor chip to the protective layer; and

wherein the electrodes of the semiconductor chip are electrically connected with the interconnect pattern.

According to this aspect of the present invention, since the adhesive is provided to extend over the protective layer, no gap is formed between the adhesive and the protective layer, the interconnect pattern is not exposed, and migration can be prevented.

(22) In this semiconductor device, conductive particles may be dispersed in the adhesive to form an anisotropic conductive material.

By means of this, since the interconnect pattern and electrodes are electrically connected by the anisotropic conductive material, the reliability and productivity are excellent.

(23) In this semiconductor device, the anisotropic conductive material may be provided to cover the whole of the interconnect pattern.

(24) In this semiconductor device, the adhesive may cover at least a part of a lateral surface of the semiconductor chip.

By means of this, since the adhesive covers at least a part of the lateral surface of the semiconductor chip, the semiconductor chip is protected from mechanical damage. Moreover, since the semiconductor chip is covered by the adhesive up to a position distant from the electrodes, water is impeded from reaching the electrodes, and corrosion of the electrodes can be prevented.

(25) In this semiconductor device, the adhesive may include a shading material.

By means of this, since the adhesive includes a shading material, light can be prevented from reaching the surface of the semiconductor chip having the electrodes. Therefore, malfunction of the semiconductor chip can be prevented.

(26) In this semiconductor device, the protective layer may be provided to cover the substrate except a region of mounting of the semiconductor chip and the periphery of the mounting region.

(27) A semiconductor device according to the present invention is manufactured by the above-described method.

(28) On a circuit board according to the present invention, the above-described semiconductor device is mounted.

(29) An electronic instrument according to the present invention has the above-described circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1D show a method of manufacturing a semiconductor device in accordance with a first reference

technique relating to the present invention;

Figs. 2A and 2B show a modification of the first reference technique;

Figs. 3A and 3B show a method of manufacturing a semiconductor device in accordance with a second reference technique relating to the present invention;

Figs. 4A and 4B show a method of manufacturing a semiconductor device in accordance with an embodiment of the present invention;

Figs. 5A and 5B show a method of manufacturing a semiconductor device in accordance with a third reference technique relating to the present invention;

Fig. 6 shows a circuit board on which is mounted a semiconductor device in accordance with the embodiment of the present invention; and

Fig. 7 shows an electronic instrument having a circuit board on which is mounted a semiconductor device in accordance with the embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

A preferred embodiment of the present invention will be described, with reference to the drawings. An embodiment of the present invention is shown in Figs. 4A and 4B. There are also some reference techniques which can be applied to the embodiment of the present invention.

First Reference Technique

A method of manufacturing a semiconductor device in accordance with the first reference technique is shown in Figs. 1A to 1D. In this reference technique, a substrate 12 is used which has an interconnect pattern 10 formed on at least one surface 18, as shown in Fig. 1A.

The substrate 12 may be a flexible substrate formed of an organic material, a metal substrate formed of an inorganic material, or a combination of these. As a flexible substrate may be used a tape carrier. If the electric conductivity of the substrate 12 is high, an insulating film is formed between the substrate 12 and the interconnect pattern 10 and on inner surfaces of through holes 14. In addition, the insulating film may also be formed on a surface of the substrate opposite to the surface on which the interconnect pattern 10 is formed.

The through holes 14 are formed in the substrate 12, and the interconnect pattern 10 is formed on the substrate, covering the through holes 14. Lands 17 for external electrodes are formed over the through holes 14, as part of the interconnect pattern 10.

An anisotropic conductive material 16, as one example of an adhesive, is provided on a thus obtained substrate 12. In the description that follows, an anisotropic conductive material is given as an example of an adhesive. The anisotropic conductive material 16 comprises an adhesive (binder) in which are dispersed conductive particles (conductive filler), and in some cases a dispersant is added. The anisotropic conductive material 16 could be previously formed as a sheet that is affixed

to the substrate 12, or it could equally well be provided as a liquid on the substrate 12. The anisotropic conductive material 16 may be provided to be larger than a surface 24 of a semiconductor chip 20 on which electrodes 22 are provided, or may be provided in a quantity to be smaller than the surface 24, then compressed so as to spread out beyond the surface 24.

Alternatively, the anisotropic conductive material 16 may be provided on the surface 24 of the semiconductor chip 20, in a quantity to be compressed so as to spread out beyond the surface 24. It should be noted that even if an adhesive not including conductive particles is used, the electrodes 22 and interconnect pattern 10 can be electrically connected.

In this reference technique, a thermosetting adhesive is used as the anisotropic conductive material, and the anisotropic conductive material 16 may further include a shading material. As a shading material can be used, for example, a black dye or black pigment dispersed in an adhesive resin.

As the adhesive may be used a thermosetting adhesive as typified by an epoxy type, or a photocurable adhesive as typified by an epoxy or acrylate type. Further, the type of adhesive cured by electron beam, or a thermoplastic (thermal adhesion) type of adhesive may equally be used. In the following description, if an adhesive other than thermosetting is used, the provision of energy should be substituted in place of the application of heat or pressure.

Next, the semiconductor chip 20 is mounted on the anisotropic conductive material 16, for example. In more detail,

the semiconductor chip 20 is mounted such that the surface 24 of the semiconductor chip 20 on which the electrodes 22 are formed faces the anisotropic conductive material 16. Moreover, the semiconductor chip 20 is disposed so that the each electrode 22 is positioned over a land (not shown in the figures) for connection of the electrodes to the interconnect pattern 10. It should be noted that the semiconductor chip 20 may have the electrodes 22 formed on two edges only, or may have the electrodes 22 formed on four edges. The electrodes 22 are commonly in the form of projections made of gold, solder or the like provided on aluminum pads. The electrodes 22 may be formed on the interconnect pattern 10 side in the form of such projections or projections formed by etching the interconnect pattern 10.

By means of the above process, the anisotropic conductive material 16 is positioned between the surface 24 of the semiconductor chip 20 on which the electrodes 22 are formed and the surface 18 of the substrate 12 on which the interconnect pattern 10 is formed. A jig 30 is then used to press a surface 26 of the semiconductor chip 20 which is opposite to the surface 24 on which the electrodes 22 are formed such that the semiconductor chip 20 is subjected to pressure in the direction of the substrate 12. Alternatively, pressure may be applied between the semiconductor chip 20 and the substrate 12. Even if the anisotropic conductive material 16 as an adhesive is provided within the area of the surface 24 of the semiconductor chip 20, the applied pressure causes it to spread out beyond

the surface 24. The jig 30 has an internal heater 32, and applies heat to the semiconductor chip 20. It should be noted that considering the requirement as far as possible to apply heat also to the spread out portion of the anisotropic conductive material 16, the jig 30 used preferably has a greater plan area than the plan area of the semiconductor chip 20. In this way, heat can easily be applied to the periphery of the semiconductor chip 20.

Thus, as shown in Fig. 1B, the electrodes 22 of the semiconductor chip 20 and the interconnect pattern 10 are electrically connected through the conductive particles of the anisotropic conductive material 16. According to this reference technique, since the interconnect pattern 10 and electrodes 22 are electrically connected through the anisotropic conductive material 16, a semiconductor device can be manufactured by a method of excellent reliability and productivity.

Since heat is applied to the semiconductor chip 20 by the jig 30, the anisotropic conductive material 16 is cured in the region of contact with the semiconductor chip 20. In the region not contacting the semiconductor chip 20 or the region apart from the semiconductor chip 20, heat does not reach the anisotropic conductive material 16, so that the curing is incomplete. The curing of these regions is carried out in the following step.

As shown in Fig. 1C, solder 34 is provided within and around the periphery of the through holes 14 in the substrate 12. A cream solder or the like may be used to form the solder

34 by printing. Alternatively, pre-formed solder balls may be mounted in the above-described position.

The solder 34 is then heated in a reflow step, and solder balls 36 are formed as shown in Fig. 1D. The solder balls 36 function as external electrodes. In this reflow step, not only the solder 34 but also the anisotropic conductive material 16 is heated. This heat cures the regions of the anisotropic conductive material 16 which are not yet cured. That is to say, of the anisotropic conductive material 16, the region not contacting the semiconductor chip 20 or the region apart from the semiconductor chip 20, is cured in the reflow step of forming the solder balls 36.

In the thus obtained semiconductor device 1, since the whole of the anisotropic conductive material 16 is cured, the possibility of the anisotropic conductive material 16 around the semiconductor chip 20 coming apart from the substrate 12 and allowing the ingress of water, leading to migration of the interconnect pattern 10 is prevented. Since the whole of the anisotropic conductive material 16 is cured, the inclusion of water within the anisotropic conductive material 16 can also be prevented.

Further in the semiconductor device 1, since the electrodes 22 provided on the surface 24 of the semiconductor chip 20 are covered by the anisotropic conductive material 16 which includes a shading material, light can be prevented from reaching this surface 24. Therefore, malfunction of the semiconductor chip 20 can be prevented.

Figs. 2A and 2B show modifications of the first reference technique. In these modifications, the structure which is the same as in the first reference technique is indicated by the same reference numerals, and description of this structure and the effect of this structure is omitted. The same is true for the following.

The step shown in Fig. 2A can be carried out after the step of Fig. 1B and before the step of Fig. 1C. In more detail, of the anisotropic conductive material 16, the region not contacting the semiconductor chip 20 and the region apart from the semiconductor chip 20, are heated by a heating jig 38. The heating jig 38 is preferably provided with a nonadhesive layer 39 formed of Teflon or the like having high nonadhesive properties to the anisotropic conductive material 16 that is an example of an adhesive, so that uncured anisotropic conductive material 16 does not adhere thereto. Alternatively, the nonadhesive layer 39 may be provided on the anisotropic conductive material 16 that is an example of an adhesive. Further, the anisotropic conductive material 16 as an example of an adhesive may be heated by a non-contact method. By this means, of the anisotropic conductive material 16, the region not contacting the semiconductor chip 20 and the region apart from the semiconductor chip 20 can be cured. In place of a jig, a hot air blower or optical heater capable of localized heating may be used.

Alternatively, as shown in Fig. 2B, after the step of Fig. 1B and before the step of Fig. 1C, a reflow step may be carried

out to electrically connect an electronic component 40 distinct from the semiconductor chip 20 to the interconnect pattern 10. By means of this reflow step, of the anisotropic conductive material 16, the region not contacting the semiconductor chip 20 and the region apart from the semiconductor chip 20 is heated and cured. It should be noted that as the electronic component 40 may be cited for example a resistor, capacitor, coil, oscillator, filter, temperature sensor, thermistor, varistor, variable resistor, or a fuse.

According to these modifications, all of the anisotropic conductive material 16 can be cured, and the possibility of the anisotropic conductive material 16 coming apart from the substrate 12 and allowing the ingress of water, leading to migration of the interconnect pattern 10 can be prevented. Since the whole of the anisotropic conductive material 16 is cured, the inclusion of water can also be prevented.

After the above described steps, the substrate 12 may be cut in the region in which the anisotropic conductive material 16 being an example of an adhesive spreads beyond the semiconductor chip 20.

This reference technique has been described with a substrate with interconnects on one surface only as the substrate 12, but is not limited to this, and a double-sided interconnect substrate or multi-layer interconnect may be used. In this case, in stead of disposing solder in the through holes, solder balls may be formed on lands provided on the surface opposite to that on which the semiconductor chip is mounted.

In place of solder balls other conductive projections may be used. The connection between the semiconductor chip and the substrate may be carried out by wire bonding. These observations apply equally to the following.

In this reference technique, not only a thermosetting adhesive, but also an anisotropic conductive material 16 being an example of a thermoplastic adhesive may be used. A thermoplastic adhesive can be hardened by cooling. Alternatively, an adhesive which can be hardened by radiation such as ultraviolet may be used. This applies equally to the following.

Second Reference Technique

A method of manufacturing a semiconductor device in accordance with the second reference technique is shown in Fig. 3A and 3B. This reference technique is carried out following on from the first reference technique.

More specifically, in this reference technique, following on from the step of Fig. 1D, the anisotropic conductive material 16 and substrate 12 are held by a fixed blade 41, and cut by a movable blade 42 to a size slightly larger than the semiconductor chip 20, as shown in Fig. 3A, yielding a semiconductor device 2 shown in Fig. 3B. The cutting means is not limited thereto, and any other available cutting means and holding means can be applied. Since the substrate 12 is cut together with the anisotropic conductive material 16, the cut through the two is coplanar, and the entire surface of the

substrate 12 is covered by the anisotropic conductive material 16. Therefore, the interconnect pattern 10 is not exposed, and moisture is prevented from reaching the interconnect pattern 10 and causing migration.

According to this reference technique, since the anisotropic conductive material 16 is cut, it does not require to be previously cut to the same size as the semiconductor chip 20 or slightly larger, and accurate positioning with respect to the semiconductor chip 20 is not required.

It should be noted that this reference technique is an example of the anisotropic conductive material 16 and substrate 12 being cut after the solder balls 36 are formed, but the timing of the cut is independent of the formation of the solder balls 36, as long as it is at least after the semiconductor chip 20 has been mounted on the anisotropic conductive material 16. However, the anisotropic conductive material 16 is preferably cured at least in the region of contact with the semiconductor chip 20. In this case, mispositioning of the semiconductor chip 20 and interconnect pattern 10 can be prevented. If the anisotropic conductive material 16 is cured rather than uncured in the location of the cut, the cutting operation will be easier.

It should be noted that when the substrate 12 is cut, the whole of the anisotropic conductive material 16 being an example of an adhesive may be cured in a single operation. For example, when the electrodes 22 of the semiconductor chip 20 and the interconnect pattern 10 are electrically connected, heat may be applied or cooling applied to the whole of the anisotropic

conductive material 16 being an example of an adhesive. When a thermosetting adhesive is used, a jig may be used which contacts both of the semiconductor chip 20 and the adhesive spreading out beyond the semiconductor chip 20. Alternatively, heating may be applied by means of an oven.

Embodiment

A method of manufacturing a semiconductor device in accordance with one embodiment of the present invention is shown in Figs. 4A and 4B. In this reference technique, the substrate 12 of the first reference technique is used, and on the substrate 12 is formed a protective layer 50. The protective layer 50 is such as to cover the interconnect pattern 10, preventing contact with water, and for example solder resist may be used.

The protective layer 50 is formed around a region 52 that is larger in extent than the region in which the semiconductor chip 20 is mounted on the substrate 12. That is to say, the region 52 is larger than the surface 24 of the semiconductor chip 20 having the electrodes 22, and within this region 52 the lands (not shown in the drawings) for connection to the electrodes 22 of the semiconductor chip 20 are formed on the interconnect pattern 10. Alternatively, the protective layer 50 may be formed to avoid at least portions for electrical connection to the electrodes 20 of the semiconductor chip 20.

On such a substrate 12 an anisotropic conductive material 54 (adhesive) of a material which can be selected as the anisotropic conductive material 16 of the first reference

technique is provided. It should be noted that the anisotropic conductive material 54 does not necessarily contain a shading material, but if it does contain a shading material then the same effect as in the first reference technique is obtained.

In this embodiment, the anisotropic conductive material 54 is provided from the region of mounting of the semiconductor chip 20 to the protective layer 50. That is to say, the anisotropic conductive material 54 covers the interconnect pattern 10 and substrate 12 in the region 52 in which the protective layer 50 is not formed, and is also formed to overlap the edge of the protective layer 50 surrounding the region 52. Alternatively, the anisotropic conductive material 54 being an example of an adhesive may be provided on the semiconductor chip 20 side. In more detail, the description in the first reference technique applies.

The semiconductor chip 20 is then pressed toward the substrate 12 and heat is applied by the jig 30, as shown in Fig. 4A. Alternatively, pressure is applied at least between the semiconductor chip 20 and the substrate 12. In this way, the electrodes 22 of the semiconductor chip 20 and the interconnect pattern 10 are electrically connected, as shown in Fig. 4B. Thereafter, in the same way as in the steps shown in Figs. 1C and 1D, solder balls are formed, and the semiconductor device is obtained.

According to this embodiment, the anisotropic conductive material 54 is not only formed in the region 52 in which the protective layer 50 is not formed, but also formed to overlap

the edge of the protective layer 50 surrounding the region 52. Consequently, there is no gap between the anisotropic conductive material 54 and the protective layer 50, and the interconnect pattern 10 is not exposed, so that migration can be prevented.

It should be noted that in this embodiment, it is preferable that the anisotropic conductive material 54 is cured also in the region spreading beyond the semiconductor chip 20. This curing step can be carried out in the same way as in the first reference technique.

Third Reference Technique

A method of manufacturing a semiconductor device in accordance with the third reference technique is shown in Figs. 5A and 5B. In this reference technique, the substrate 12 of the first reference technique is used, and an anisotropic conductive material 56 (adhesive) is provided on the substrate 12. The difference between this reference technique and the first reference technique is in the thickness of the anisotropic conductive material 56. That is to say, as shown in Fig. 5A, in this reference technique the thickness of the anisotropic conductive material 56 is greater than the thickness of the anisotropic conductive material 16 shown in Fig. 1A. More specifically, the anisotropic conductive material 56 is thicker than the interval between the surface 24 of the semiconductor chip 20 having the electrodes 22 and the interconnect pattern 10 formed on the substrate 12. The anisotropic conductive

material 56 is at least slightly larger than the semiconductor chip 20. It should be noted that it is sufficient for either of these thickness and size conditions to be satisfied.

As shown in Fig. 5A, the semiconductor chip 20 is then pressed toward the substrate 12 and heat is applied by the jig 30, for example. By doing this, the anisotropic conductive material 56 surrounds a part or all of a lateral surface 28 of the semiconductor chip 20, as shown in Fig. 5B. Thereafter, solder balls are formed in the same way as in the steps shown in Figs. 1C and 1D, and the semiconductor device is obtained.

According to this reference technique, since at least part of the lateral surface 28 of the semiconductor chip 20 are covered by the anisotropic conductive material 56, the semiconductor chip 20 is protected from mechanical damage. Moreover, since the anisotropic conductive material 56 covers as far as a position removed from the electrodes 22, corrosion of the electrodes 22 and so on can be prevented.

Although the above embodiment has been described principally in terms of a chip size/scale package (CSP) of face-down bonding (FDB), the present invention can be applied to any semiconductor device to which FDB is applied, such as a semiconductor device to which Chip on Film (COF) or Chip on Board (COB) is applied, or the like.

A circuit board 1000 on which is mounted a semiconductor device 1100 fabricated by the method of the above described embodiment is shown in Fig. 6. An organic substrate such as a glass epoxy substrate or the like is generally used for the

circuit board 1000. On the circuit board 1000, an interconnect pattern of for example copper is formed to provide a desired circuit. Then electrical connection is achieved by mechanical connection of the interconnect pattern and external electrodes of the semiconductor device 1100.

It should be noted that the semiconductor device 1100 has a mounting area which can be made as small as the area for mounting a bare chip, and therefore when this circuit board 1000 is used in an electronic instrument, the electronic instrument itself can be made more compact. Moreover, a larger mounting space can be obtained within the same area, and therefore higher functionality is possible.

Then as an example of an electronic instrument equipped with this circuit board 1000, a notebook personal computer 1200 is shown in Fig. 7.

It should be noted that, whether active components or passive components, the present invention can be applied to various surface-mounted electronic components. As electronic components, for example, may be cited resistors, capacitors, coils, oscillators, filters, temperature sensors, thermistors, varistors, variable resistors, and fuses.

CLAIMS

1. A method of manufacturing a semiconductor device in which a semiconductor chip on which electrodes are formed, and a substrate on which an interconnect pattern is formed and which is covered by a protective layer except a region in said interconnect pattern of electrical connection with said electrodes, are connected by an adhesive, said method comprising:

a first step of providing said adhesive on said substrate from a region of mounting of said semiconductor chip to said protective layer, between said interconnect pattern and said electrodes; and

a second step of adhering said substrate to said semiconductor chip by means of said adhesive to electrically connect said interconnect pattern with said electrodes.

2. The method of manufacturing a semiconductor device as defined in claim 1,

wherein said interconnect pattern and said electrodes are electrically connected by conductive particles dispersed in said adhesive.

3. The method of manufacturing a semiconductor device as defined in claim 1,

wherein before said first step, said adhesive is previously disposed on the surface of said semiconductor chip

on which said electrodes are formed.

4. The method of manufacturing a semiconductor device as defined in claim 1,

wherein before said first step, said adhesive is previously disposed on the surface of said substrate on which said interconnect pattern is formed.

5. The method of manufacturing a semiconductor device as defined in claim 1, wherein said adhesive is a thermosetting adhesive.

6. The method of manufacturing a semiconductor device as defined in claim 5,

wherein said adhesive is spread out beyond said semiconductor chip in said first step; and

wherein heat is applied between said semiconductor chip and said substrate to cure said adhesive between said semiconductor chip and said substrate in said second step;

said manufacturing method further comprising a third step of applying heat to a part of said adhesive not completely cured in said second step.

7. The method of manufacturing a semiconductor device as defined in claim 6, wherein said adhesive is heated by means of a heating jig in said third step.

8. The method of manufacturing a semiconductor device as defined in claim 7,

wherein a nonadhesive layer having improved nonadhesive properties with respect to said adhesive is interposed between said heating jig and said adhesive, before heating said adhesive.

9. The method of manufacturing a semiconductor device as defined in claim 8, wherein said nonadhesive layer is provided on said heating jig.

10. The method of manufacturing a semiconductor device as defined in claim 8, wherein said nonadhesive layer is provided on said adhesive.

11. The method of manufacturing a semiconductor device as defined in claim 6, wherein said adhesive is heated by a non-contact method in said third step.

12. The method of manufacturing a semiconductor device as defined in claim 6,

further comprising a reflow step of forming solder balls on said substrate to be connected to said interconnect pattern,

wherein said third step is carried out in said reflow step.

13. The method of manufacturing a semiconductor device as

defined in claim 6,

further comprising a reflow step of electrically connecting an electronic component other than said semiconductor chip to said interconnect pattern,

wherein said third step is carried out in said reflow step.

14. The method of manufacturing a semiconductor device as defined in claim 1,

wherein said substrate is cut together with said adhesive in a region not in contact with said semiconductor chip, after said second step.

15. The method of manufacturing a semiconductor device as defined in claim 14,

wherein said substrate is cut in a region outside the edge of said interconnect pattern.

16. The method of manufacturing a semiconductor device as defined in claim 14,

wherein the whole of said adhesive is cured before said substrate is cut together with said cured adhesive.

17. The method of manufacturing a semiconductor device as defined in claim 1,

wherein said adhesive is caused to surround at least a part of a lateral surface of said semiconductor chip in said

second step.

18. The method of manufacturing a semiconductor device as defined in claim 17,

wherein said adhesive is provided in said first step at a thickness greater than the interval between said semiconductor chip and said substrate after said second step, and is spread out beyond said semiconductor chip by applying pressure between said semiconductor chip and said substrate in said second step.

19. The method of manufacturing a semiconductor device as defined in claim 1,

wherein said adhesive includes a shading material.

20. The method of manufacturing a semiconductor device as defined in claim 1,

wherein said substrate is provided previously covered by said protective layer except a region of mounting of said semiconductor chip and the periphery of said mounting region.

21. A semiconductor device comprising:

a semiconductor chip having electrodes; a substrate on which an interconnect pattern is formed; a protective layer provided on said substrate excluding a region of said interconnect pattern of electrical connection with said electrodes of said semiconductor chip; and an adhesive;

wherein said adhesive is provided on said substrate from a region of mounting of said semiconductor chip to said protective layer; and

wherein said electrodes of said semiconductor chip are electrically connected with said interconnect pattern.

22. The semiconductor device as defined in claim 21,

wherein conductive particles are dispersed in said adhesive to form an anisotropic conductive material.

23. The semiconductor device as defined in claim 22,

wherein said anisotropic conductive material is provided to cover the whole of said interconnect pattern.

24. The semiconductor device as defined in claim 21,

wherein said adhesive covers at least a part of a lateral surface of said semiconductor chip.

25. The semiconductor device as defined in claim 21,

wherein said adhesive includes a shading material.

26. The semiconductor device as defined in claim 21,

wherein said protective layer is provided to cover said substrate except a region of mounting of said semiconductor chip and the periphery of said mounting region.

27. A semiconductor device manufactured by the method as

defined in any of claims 1 to 20.

28. A circuit board on which is mounted the semiconductor device as defined in any of claims 21 to 26.

29. An electronic instrument having the circuit board as defined in claim 28.

ABSTRACT

A method of manufacturing a semiconductor device in which is provided a substrate 12 on which an interconnect pattern 10 is formed and which is covered by a protective layer 50 except a region of electrical connection with electrodes 22 of a semiconductor chip 20, the method comprising: a first step of providing an anisotropic conductive material 16 on the substrate 12 from a region of mounting of the semiconductor chip 20 to the protective layer 50, between the interconnect pattern 10 and the electrodes 22; and a second step of adhering the substrate 12 to the semiconductor chip 20 by means of the anisotropic conductive material 16 to electrically connect the interconnect pattern 10 with the electrodes 22.

FIG.1A

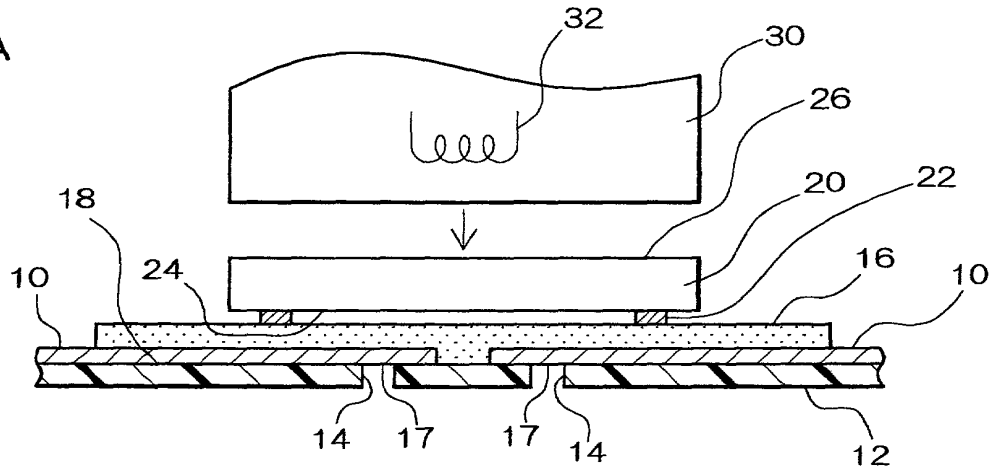


FIG.1B

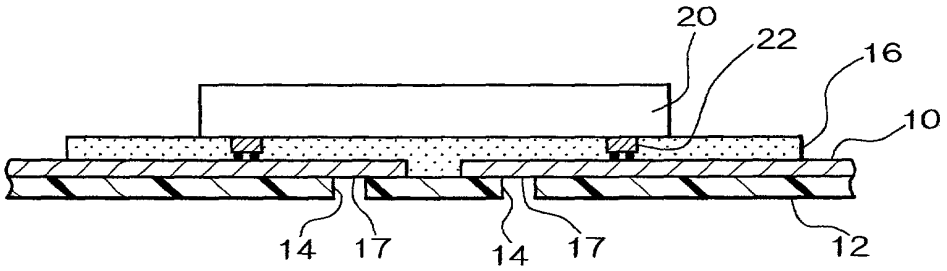


FIG.1C

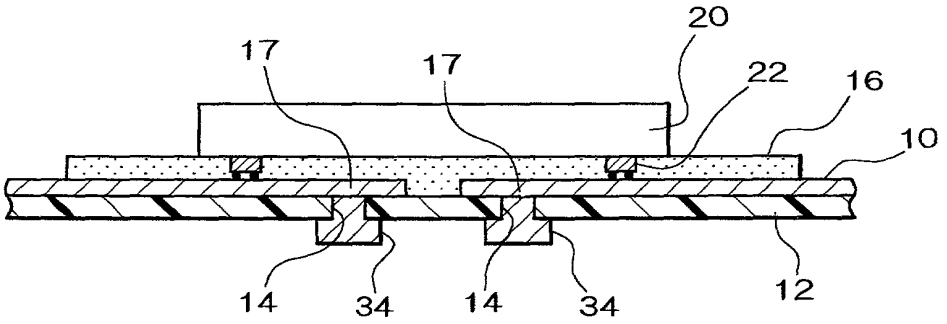


FIG.1D

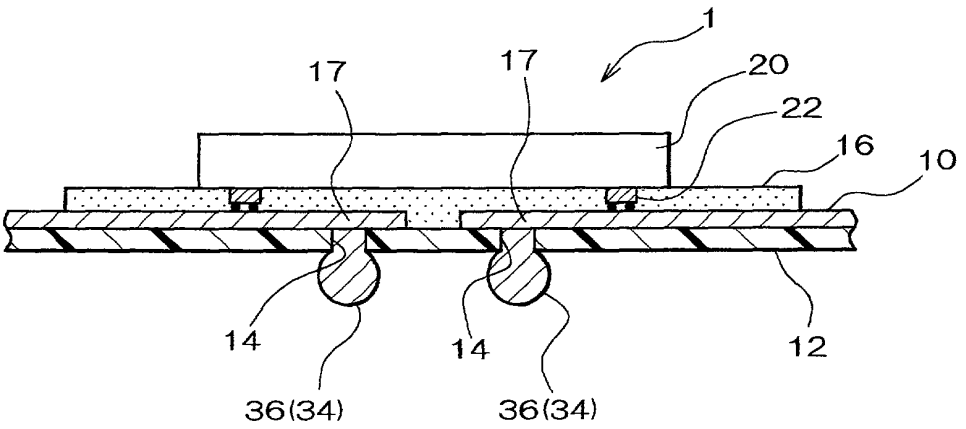


FIG.2A

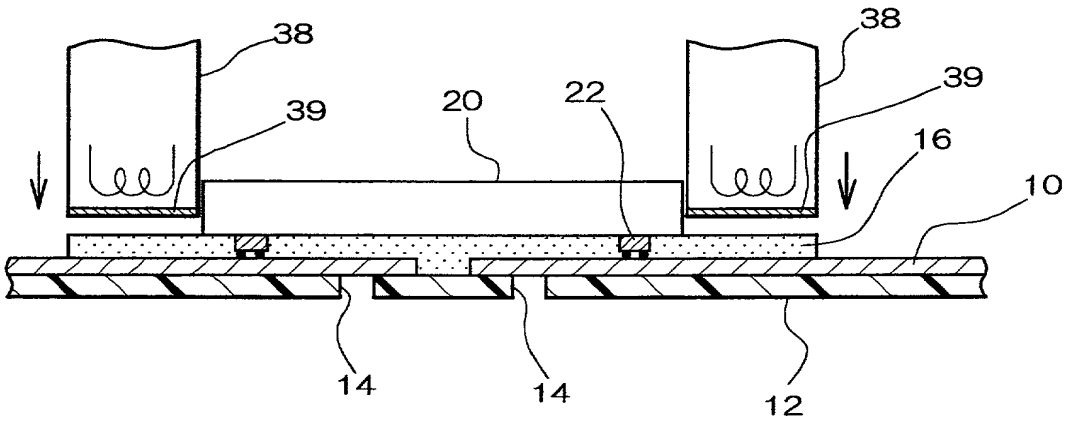


FIG.2B

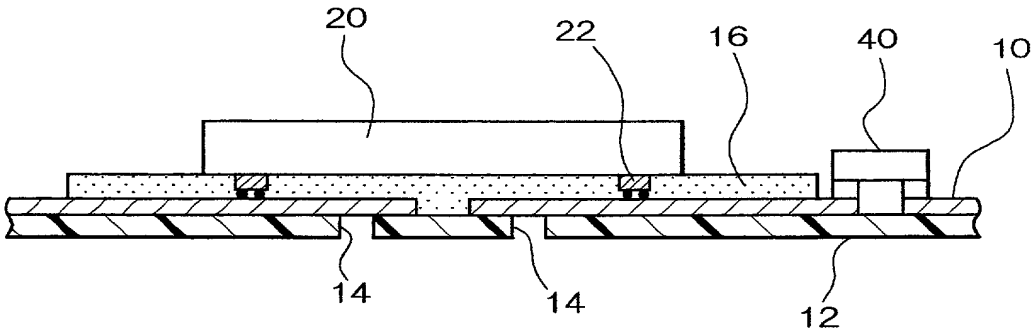


FIG.3A

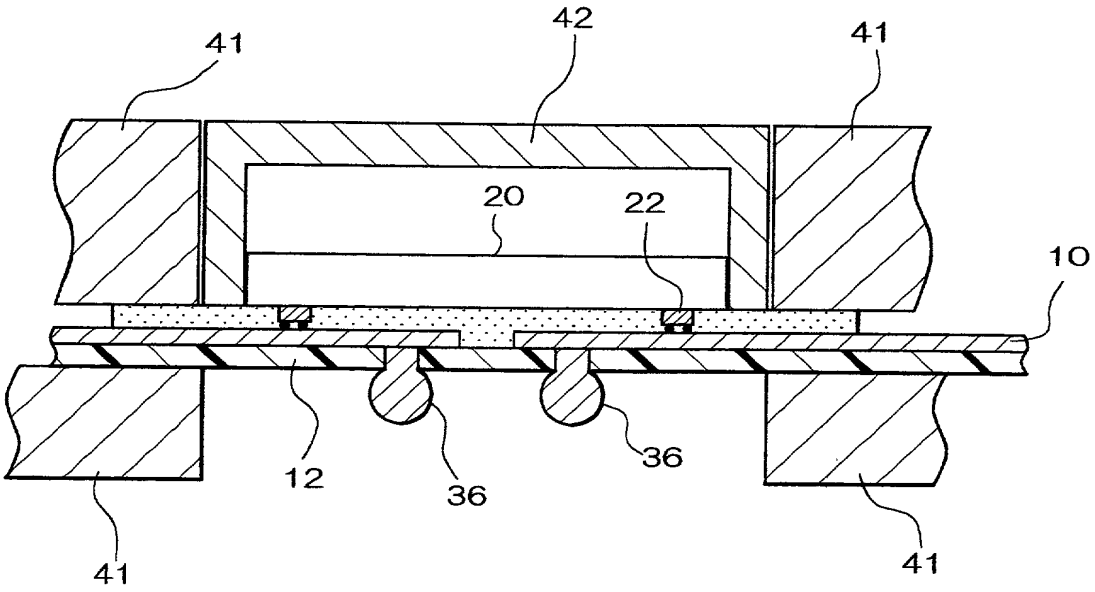


FIG.3B

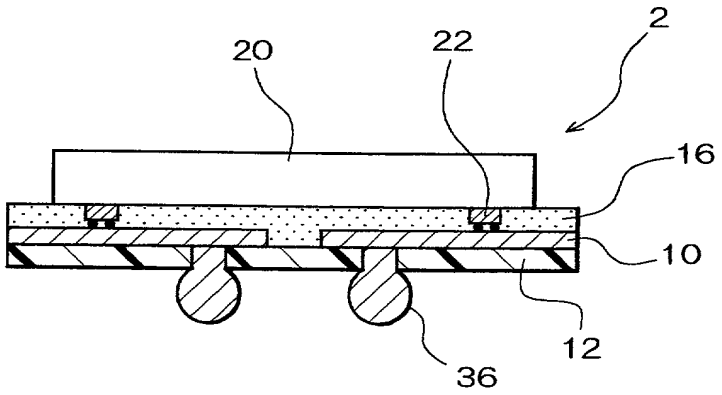


FIG.4A

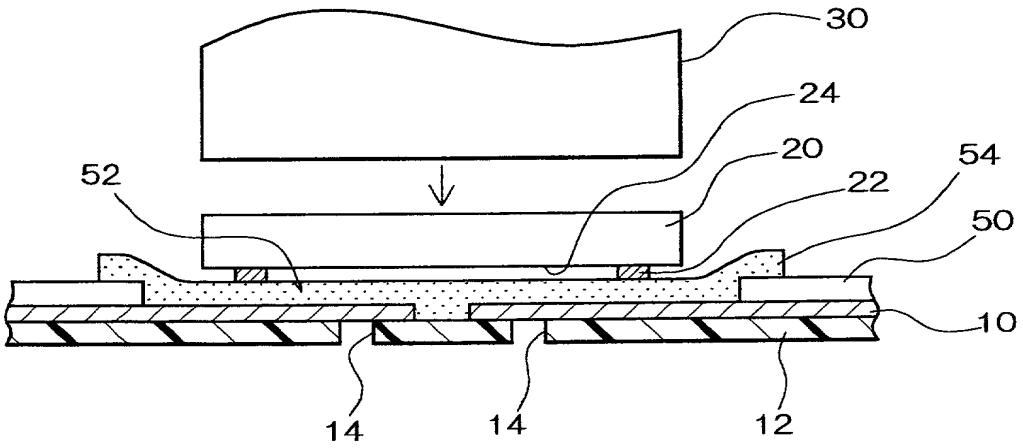


FIG.4B

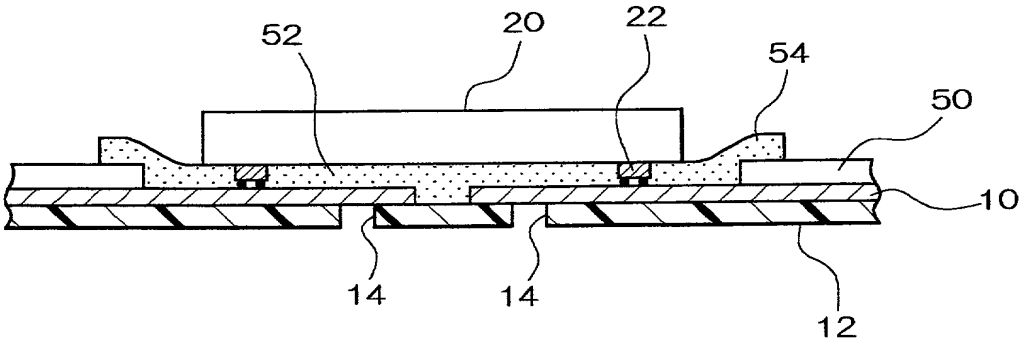


FIG.5A

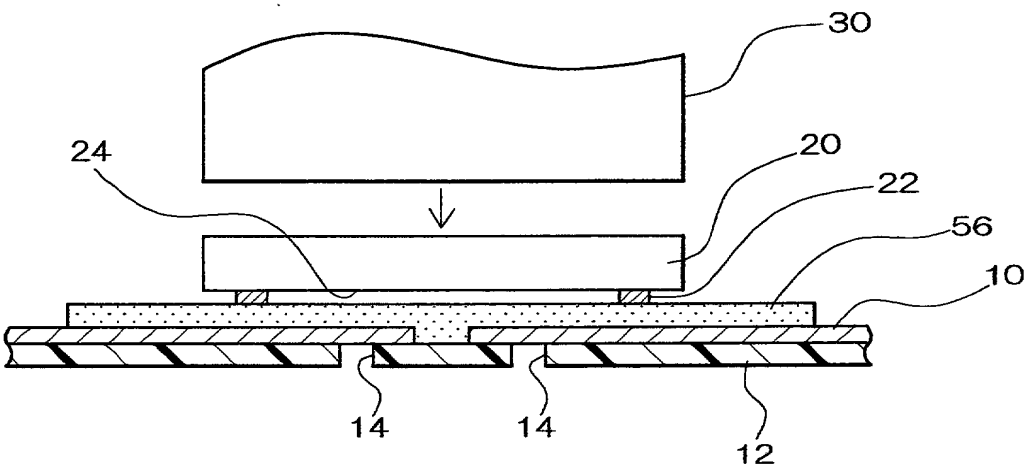


FIG.5B

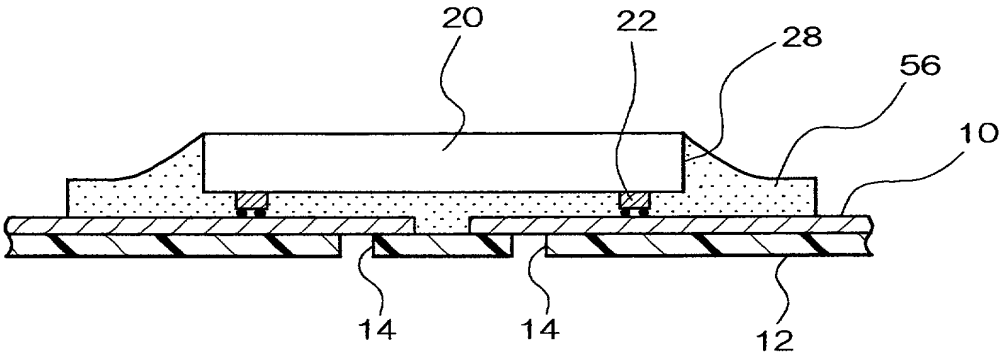


FIG.6

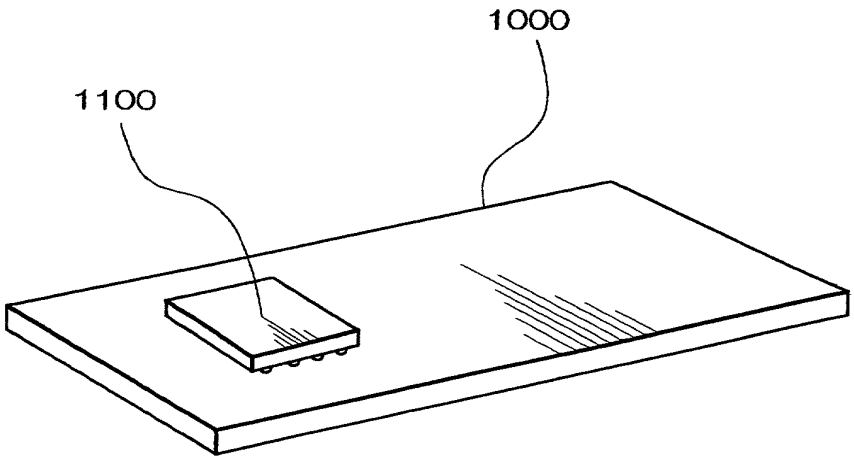
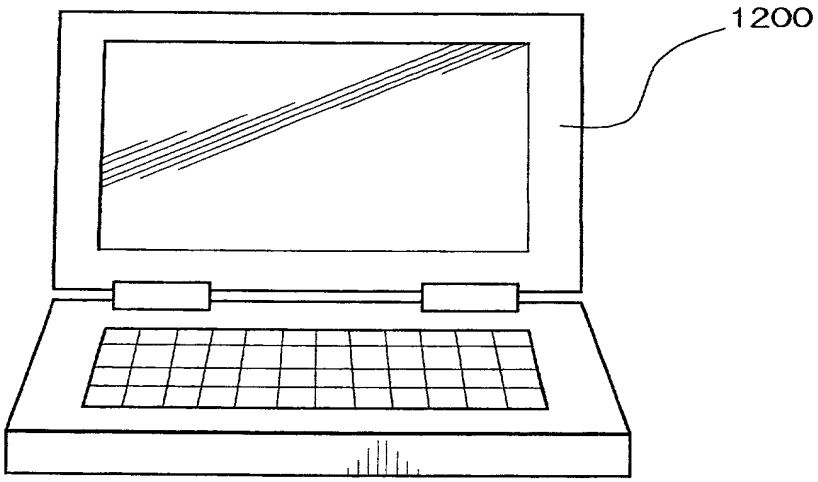


FIG.7



PTO/SB/106 (8-96)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to collection of information unless it displays a valid OMB control number.

Seiko Epson Ref. No.: F004527US00 Attorney's Ref. No.: 105029

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

半導体装置及びその製造方法、回路基板並びに電子機器

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☒ 1999年6月25日に提出され、米国出願番号または特許協定条約 国際出願番号をPCT/JP99/03417 とし、（該当する場合） _____ に訂正されました。

☒ was filed on June 25, 1999 as United States Application Number or PCT International Application Number PCT/JP99/03417 and was amended on _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

PTO/SB/106 (8-96)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条（ａ）-（ｄ)項又は３６５条(ｂ)項に基き下記の、米国以外の国の少なくとも１ヶ国を指定している特許協力条約３６５条(ａ)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
10-201246	Japan	01/July/1998	☐
			☐

私は、第３５編米国法典１１９条(ｅ)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(ｃ)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
PCT/JP99/03417	25/June/1999	Pending

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/106 (8-96)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)
Caroline D. Dennison, (Reg.34,494)

書類送付先：
OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320

Send Correspondence to:
OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320

直接電話連絡先： (名前及び電話番号)
OLIFF & BERRIDGE, PLC
(703) 836-6400

Direct Telephone Calls to: *(name and telephone number)*
OLIFF & BERRIDGE, PLC
(703) 836-6400

唯一または第一発明者名
橋元 伸晃

Full name of sole or first inventor
Nobuaki HASHIMOTO

発明者の署名 日付
橋元伸晃 2000年 2月15日

Inventor's signature Date
Nobuaki Hashimoto February 15, 2000

住所
日本国, 長野県, 諏訪市

Residence
Suwa-shi, Nagno-ken, Japan

国籍
日本

Citizenship
Japan JPX

私書箱
392-8502 日本国長野県諏訪市大和3丁目3番5号
セイコーエプソン株式会社内

Post Office Address
c/o Seiko Epson Corporation
3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502 Japan

第二共同発明者

Full name of second joint inventor, if any

第二共同発明者の署名 日付

Second inventor's signature Date

住所
日本国, _____, _____

Residence
_____, _____, Japan

国籍

Citizenship

私書箱

Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)